Assignment 1

1. A machine has a 500MHz system clock. Memory takes 30 ns to access a word. How many clock cycles is this?

2. A machine has a base CPI of 2 clock cycles. Measurements obtained show that the instruction miss rate is 8% and the data miss rate is 10%, and that on average, 30% of all instructions contain one data reference. The miss penalty for the cache is 16 cycles. What is the total CPI?

3. Draw a picture showing the organization of a direct-mapped cache with 8 four-byte words per block, with a capacity of 128KB. Show any multiplexors, gates, needed. Show how a 32-bit physical byte address is mapped into the cache.

4. This question has three parts, based on the following sequence of ***word addresses*** generated by the processor:

   1, 134, 212, 1, 135, 213, 162, 161, 2, 44, 41, 221

   (a) Given a direct-mapped cache with 16 one-word blocks that is initially empty, identify the binary address, the tag, and the index, and then label each reference as a hit or a miss and show the final contents of the cache.

   (b) Do the same thing as in part a, except this time assume that the cache has eight two-word blocks.

5. Assume that in a particular machine, arrays are stored in row-major order. Given the following code fragment:

```
for ( i = 0; i < 8000; i++)
    for ( j = 0; j < 8; j++)
        a[i][j] = b[j][0] * a[j][i];
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   (a) References to which variables exhibit spatial locality?

   (b) References to which variables exhibit temporal locality?